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A RADIATION-HARD CMOS/SOS ALU,(U)
OCT 77 R A KJAR, M MARTINEZ, A E WASKIEWICZ F04704-75-C-0007
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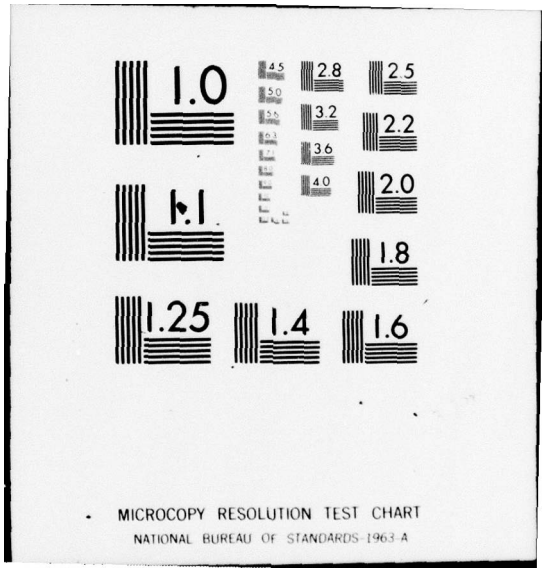
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Rockwell International

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(6) A RADIATION-HARD CMOS/SOS ALU

(12) 6 p.

(11) 5 October 1977

(10) R. A. Kjar, M. Martinez and A. E. Waskiewicz

Presented to

23rd Conference on Magnetism and
Magnetic Materials
Minneapolis, MN
8-11 November 1977

(15) F04704-75-C-0007

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A RADIATION-HARD CMOS/SOS ALU*

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Abstract

A radiation-hard CMOS/SOS technology has been used to fabricate a complex LSI circuit containing over 2200 transistors. The circuit is an eight bit wide arithmetic and logic unit (ALU) slice. This paper describes the results of electrical, temperature, and radiation tests on the ALU circuit. An instruction cycle-time of less than 240 ns was achieved for nominal operation at +11V and 25° C. This time increases to 300 ns at 125°C. After irradiation to 10^6 rads (Si) under bias, operation was degraded only slightly. The 25° C and 125°C postradiation cycle times were within 320 and 360 ns, respectively. Radiation tolerance from part to part and lot to lot was excellent, thus demonstrating the applicability of radiation hard CMOS/SOS to LSI circuitry.

Introduction

Radiation-hard CMOS/SOS LSI technology has reached the maturity required to implement complex functions in a single circuit. The ALU shown in Figure 1 and described in this paper is typical of the applications for this technology. The ALU chip is 205 x 233 mils in size and contains over 2200 transistors. This chip is designed to serve as the main computational element in high-speed space and missile computers. As such, it is required to operate over a full -55° C to +125° C range as well as meet severe radiation hardness criteria.

Circuit Description

The ALU is a device which performs all the standard arithmetic and logic functions normally associated with computer arithmetic. It is designed to function as the key element of a central processor unit (CPU). This design is implemented as an eight-bit slice with all the necessary inputs and outputs to allow cascading to form a 32-bit unit. The major components of the device are identified in Figure 2.

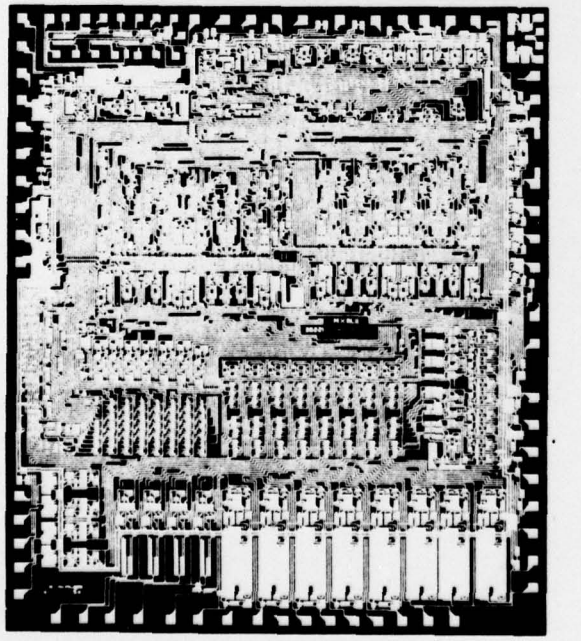


Figure 1. CMOS/SOS ALU

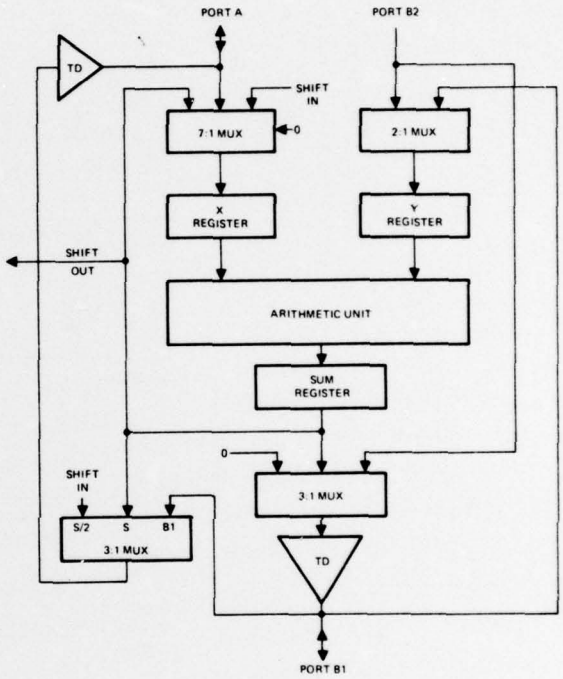


Figure 2. Internal Organization of ALU

One of the features of the overall CPU is the tri-state bidirectional bus, which is the main data path. This data bus requires the ALU chip to have a bidirectional port (Port B1) with tri-state drivers capable of driving 100 pf loads. The architecture requires that the ALU have two additional ports to communicate with other devices. One of these ports is strictly an input port to provide the ALU with operands (Port B2). The second port is another tri-state bidirectional data port (Port A); however, the associated drivers only have to accommodate 10 pf loads. Tri-state drivers are used to provide maximum system flexibility and also to allow a common pin to be used for input and output.

Since Port B1 is often used for transporting data unrelated to the computation being performed in the ALU, the ALU must have inter-chip shift paths that are independent of Port B1. The requirements for division, and for the two-bit-at-a-time multiply algorithms, dictate four shift inputs and four shift outputs for each ALU chip. However, since the shift outputs need only drive the next shift inputs, the drivers can be small.

Transmission gate multiplexers (MUX's) are provided on all input and output ports. Multiplexers on the input allow for selection of inputs and also provide shift paths for implementing division and two-bit-at-a-time multiply algorithms. Shift information is obtained from a higher order device (for functions such as multiply), or from a lower order device

*This work was sponsored by the USAF Space and Missile Systems Organization under Contract No. F04704-75-C-0007. The Project Officer is Captain R. R. Warzynski.

(for functions such as divide). Multiplexers on the output nodes allow various internal paths to be selected for providing inputs.

The multiplexers feed into clocked input buffer registers (mechanized with transmission gates). These clocked registers, along with logic-controlled registers, are used extensively in both the control and the arithmetic sections. These latches allow internal synchronization of controls and operands as well as system synchronization. Timing for the clocked registers is provided by a single-logic-level clock input.

Five input signals are decoded to generate the necessary control signals. Decoding of these arithmetic and logic function control lines takes place before the buffer registers are opened; therefore, their decode time is eliminated from the critical time delay path. Table 1 lists the arithmetic and logical operations that the ALU can perform.

Table 1. ALU Arithmetic and Logical Functions

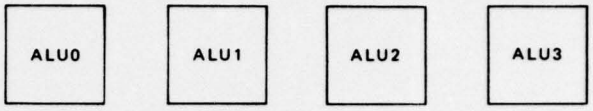
• LOGICAL AND	$S = X \cdot Y$
• LOGICAL OR	$S = X + Y$
• LOGICAL EXCLUSIVE OR	$S = X \oplus Y$
• ZERO	$S = 0$
• ADD	$S = X + Y$
• ADD AND INCREMENT	$S = X + Y + 1$
• SUBTRACT	$S = X - Y$
• SUBTRACT AND DECREMENT	$S = X - Y - 1$
• *DIVIDE* LOGIC	$S = X \pm Y$
• PASS Y	$S = Y$
• INCREMENT Y	$S = Y + 1$
• 2's COMPLEMENT Y	$S = 0 - Y$
• 1's COMPLEMENT Y	$S = 0 - Y - 1 = \bar{Y}$
• PASS X	$S = X$
• INCREMENT X BY 1	$S = X + 1$
• INCREMENT X BY 2	$S = X + 2$
• DECREMENT X BY 1	$S = X - 1$
• DECREMENT X BY 2	$S = X - 2$
• ALL 1's	$S = 11111111_2$
• REMOVE EXPONENT BIAS	$S = X - 200_8$
• EXPONENT UNDERFLOW CHECK	$S = X - 040_8$

The carry structure for the device is implemented in the following manner. The internal chip carry-structure is implemented using a parallel look-ahead approach for maximum speed. However, the inter-chip carry structure uses a pass-through approach which minimizes the number of required pins.

The design includes allowance for expected changes in transistor thresholds, leakage and gain as a result of ionizing radiation dose. No other special design procedures were used. Transmission gates, for example, were used extensively in the circuit design, but the bodies of these transistors were allowed to float. P-channel transistors, thus, could and did operate at positive effective gate voltages during exposure to ionizing radiation. The effect of transient photoconduction on circuit operation was also considered in the design. Circuit configurations considered to be highly sensitive to photoconduction effects were avoided, but no attempt was made to optimize the transient radiation harness.

Electrical Performance

The performance of the ALU in a 32-bit system for a 32-bit addition can be represented as follows



The four ALU's above can be visualized as the arithmetic unit of a 32-bit CPU. They have interconnections for carries and shift signals, which are used for arithmetic operations. The worst-case delay for such a system occurs when a carry generated by the low order ALU (ALU3) must be passed by both ALU2 and ALU1 to reach ALU0.

Table 2 presents data taken from typical ALU devices. The first column shows the amount of time required for a given ALU device to generate a Carry-Out. This time is measured from an enabling clock transition.

Table 2. ALU Speed Measurements Data in ($\phi_1 - \phi_0$ Transition) to Generating Carry Out (ns)

DEVICE NO.	25°C			125°C		
	CLOCK → C_{OUT}	C_{IN} → B_1 OUT	32 BIT ADD*	CLOCK → C_{OUT}	C_{IN} → B_1 OUT	32 BIT ADD*
15	102	86	210	141.5	114.5	285
20	112	90.5	223	152.5	118	300.5
102	120.5	93.5	234	162	119.5	313.5
107	87.5	73.5	179	131	96.5	252.5
113	120	104.5	244.5	155	126.5	306.5
21	94	96.5	211.5	118	114.5	248.5
152	111.5	82.5	215	146	108	281
164	104.5	79.5	205	145	105.5	272.5
AVG	106.5	89.5	215	144	111	288

*CALCULATED FROM DELAYS FOR SINGLE CHIP

The measured amount of time required for an ALU device to pass a Carry-In signal is 8 to 12 ns at 25° C and 10 to 14 ns at 125° C.

The time required for a 32-bit addition can be computed by adding the amount of time required by ALU3 to generate a Carry (≈105 ns), to the amount of time required by ALU2 and ALU1 to pass a Carry (≈20 ns), to the amount of time required by ALU0 to generate outputs (≈90 ns). The total time required for a 32-bit addition is then about 215 ns. The last half of Table 2 shows increased propagation delays at 125° C.

Circuit Fabrication

Fabrication is performed using a CMOS/SOS self-aligned thick-oxide process. A silicon nitride mask is used to mask gate areas during diffusion of source and drain, and during growth of a thick field oxide. This process results in a self-aligned thick field oxide over source and drain regions and thus minimizes gate overlap capacitance. The gate was formed by thermal oxidation of the silicon in a steam HCl ambient.[1] Aluminum metallization was deposited by RF evaporation. A more detailed description of the circuit fabrication process and of the process parameters has been described in a previous paper.[2] Absolute radiation hardness and lot to lot repeatability, however, have improved over that previously reported. Figures 3 and 4 show the range of threshold voltage shifts, under radiation, for four consecutive ALU lots.

The threshold voltages were measured within 5 minutes of the radiation exposure and no significant annealing was

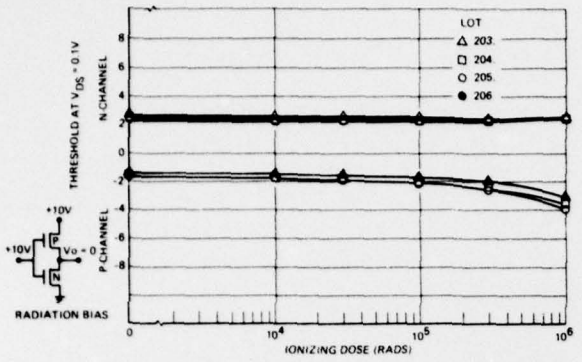


Figure 3. ALU Threshold Voltages vs Total Dose

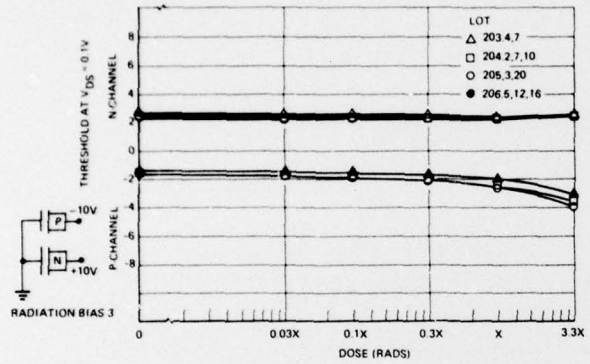


Figure 4. ALU Threshold Voltage vs. Total Dose

found to occur within that time. Each transistor type is irradiated under four bias conditions, but only the two bias conditions for which the largest radiation-induced threshold shifts occurred are shown. Radiation bias conditions, with positive gate-to-body bias on p-channel transistors, have often been reported to result in larger threshold shifts with radiation, but the data of Figure 4 show that the process used for the ALU circuits effectively controls radiation-induced threshold shifts under this worst-case bias condition.

Ionizing Radiation Dose Effects

The permanent effects of radiation on circuit operation were measured by comparing pre- and postradiation electrical characteristics of six of the CMOS/SOS ALU circuits. The primary radiation source was the Rockwell International Co^{60} gamma cell.

The circuit was statically biased during radiation, under data and control input states specifically selected to provide +10V gate-to-body bias on p-channel transistors in transmission gates (worst case).

The major effects of radiation doses to 10^6 rads (Si) were a slight increase in propagation delay times and an increase in standby power. Typical propagation delay time increases were about 20 percent at 10^6 rads (Si). Figure 5 shows the effect of radiation dose on the instruction cycle time. Data obtained from six parts, representing three fabrication lots, are shown. Standby current increased from ~200μA at 25° C pre-irradiation to 3-4 mA at 25° C, after 10^6 rads (Si).

This post-radiation standby current for the circuit is consistent with the post-radiation back-channel current measured on n-channel test transistors. The circuit requires

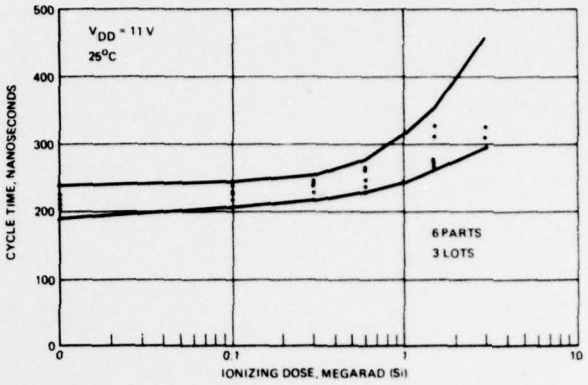


Figure 5. Instruction Cycle Time (32 Bits) as a Function of Total Ionizing Dose

30-40 mA of power supply current when operating at speed with 100 pf loads, hence the measured postradiation standby currents do not add significantly to power supply drain in an operating system.

A small sample (4) of circuits were irradiated to neutron fluences of 9×10^{13} and 3×10^{14} n/cm^2. No degradation effects beyond those attributable to the accompanying ionizing dose were observed.

Transient Radiation Effects

Circuit performance in a transient radiation environment was measured by operating the circuit during and after exposure to the radiation pulse from the Rockwell International Flash X-Ray source. The devices were operated at a frequency of 1 MHz with the radiation pulse synchronized to occur during active switching of the device logic circuitry.

A minicomputer-controlled tester was used to monitor operation of the ALU circuit, to detect errors in operation and to measure recovery time. Eleven circuits were tested with a radiation pulse width of 30 ns with the results shown in Table 3.

Table 3. Upset Level at MLU Circuit

TEST DEVICE NO.	FUNCTIONING CORRECTLY (R(Si)/SEC)	LOGIC UPSET (R(Si)/SEC)
1*	3.7×10^{10}	5.5×10^{10}
2	3.0×10^{10}	4.0×10^{10}
3	3.3×10^{10}	5.2×10^{10}
4	2.4×10^{10}	3.1×10^{10}
5	2.8×10^{10}	3.6×10^{10}
6	3.4×10^{10}	4.9×10^{10}
7	4.2×10^{10}	6.1×10^{10}
8	6.9×10^{10}	8.7×10^{10}
9	5.2×10^{10}	7.4×10^{10}
10	3.3×10^{10}	4.3×10^{10}
11	4.7×10^{10}	5.7×10^{10}

*TEST MADE AFTER 3×10^5 RADS (Si) TOTAL DOSE EXPOSURE

All circuits operated without error through a radiation level of 2.4×10^{10} rad (Si)/sec. The lowest radiation level at which logic upset occurred was 3.1×10^{10} rads (Si)/sec, and the highest level at which a circuit would operate with no error was 6.9×10^{10} rad (Si)/sec.

Radiation at higher dose rates resulted in logic upset which continued for several microseconds after the radiation pulse. Normally circuit outputs were driven to a low (OV) level during the recovery period. A full +12V logic level was not obtained until some time after functional circuit operation returned. Figure 6 shows the high-logic-state recovery with time after the radiation pulse. One circuit failed catastrophically and, hence, did not recover as shown by the continuous 12V offset level.

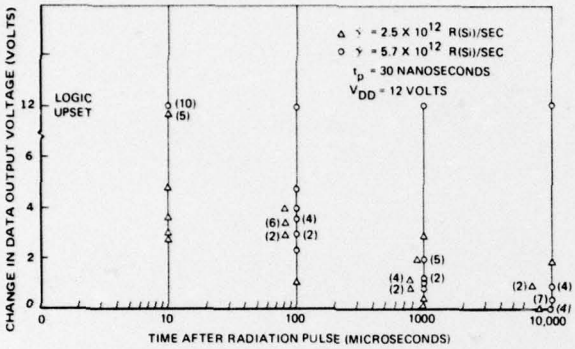


Figure 6. Change in Output Voltage as a Function of Time After Transient-Ionizing Pulse

Conclusions

A highly useful ALU circuit with greater than 10^6 rads (Si) total dose hardness has been demonstrated. Radiation effects on circuit speed and power requirements were minor and consistent with both design analysis and measured radiation effects on individual test transistors. The effect of a 10^6 rads (Si) radiation dose and 125° C ambient temperature on circuit operation were similar. Radiation, thus, becomes another environmental factor which can be anticipated and designed for as readily as the temperature environment.

The design approach use is of equal significance with the radiation hardness achieved. Transmission gates are highly useful in implementing CMOS logic but have often been avoided in radiation hard CMOS/SOS circuits because a positive gate to channel bias can occur if the gate is at V_{DD} and both input and output are at V_{SS}. The ALU circuit used approximately 200 transmission gates with no provision to avoid the positive gate-bias condition. P-channel threshold voltage shifts under this bias condition are about 2V at 10^6 rads (Si). There is no indication that the free use of transmission gates in any way reduced the radiation performance of the circuit.

Acknowledgments

The authors wish to thank Dr. T. F. Gunckel for the basic circuit concept, B. Lovinger and A. Beek for design analysis support, S. Lee, M. Morris and D. Wyckoff for circuit fabrication and T. Still for electrical performance testing of the subject circuit.

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